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57	0	703/13 and (integrated adj circuit microprocessor microcontroller) and (instruction adj set adj simulat$ iss) and (bus near model$) with hardware and loop and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:11
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60	0	703/$ and (integrated adj circuit microprocessor microcontroller) same loop and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:15
59	2	703/$ and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and loop and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:12
61	0	703/$ and (integrated adj circuit microprocessor microcontroller) same loop and (bus near model$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:15
62	6	(integrated adj circuit microprocessor microcontroller) same loop and (bus near model$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:17
65	10	703/$ and (integrated adj circuit microprocessor microcontroller) same loop same model$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:19
66	25	703/$ and (integrated adj circuit $5processor $5controller) with loop same model$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:20
67	9	703/$ and (integrated adj circuit $5processor $5controller) near3 loop same model$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:24
68	0	703/$ and (integrated adj circuit $5processor $5controller) near3 loop same hardware same model$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:26
69	4	(integrated adj circuit $5processor $5controller) near3 loop same hardware same model$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:27
70	12	(integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:31

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72	32	703/13-25.ccls. and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:33
73	0	703/13-25.ccls. and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:44
74	0	703/$ and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:34
75	1	(integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:35
76	2	(integrated adj circuit $5processor $5controller) with loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:53
78	21	703/13 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
79	21	703/14 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
80	10	703/15 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
81	11	703/16 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38

82	12	703/17 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
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84	6	703/19 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
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86	8	703/21 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
87	12	703/22 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
88	22	703/23 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
89	11	703/24 and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
77	1	703/13-25.ccls. and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:38
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95	0	703/24 and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:45
96	0	703/25 and (integrated adj circuit $5processor $5controller) near3 loop same hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:45
97	34	(integrated adj circuit $5processor $5controller) with loop and hardware same (model$ simulat$ emulat$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:53
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1 **High quality desktop video conferencing using agent based systems**
Catrava, S.;
Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on , 27-29 March 1996
Pages:37 - 43

[Abstract] [PDF Full-Text (588 KB)] **IEEE CNF**

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2 **Architectural and compiler support for energy reduction in the memory hierarchy of high performance microprocessors**
Hajj, N.B.M.; Polyckronopoulos, C.; Stamoulist, G.;
Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 10-12 Aug. 1998
Pages:70 - 75

[Abstract] [PDF Full-Text (524 KB)] **IEEE CNF**

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1 **Sunder: a programmable hardware prefetch architecture for numerical loops**
Tzi-cker Chiueh;
Supercomputing '94. Proceedings , 14-18 Nov. 1994
Pages:488 - 497

[Abstract] [PDF Full-Text (764 KB)] **IEEE CNF**

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2 **Effective hardware-based data prefetching for high-performance processors**
Tien-Fu Chen; Jean-Loup Baer;
Computers, IEEE Transactions on , Volume: 44 , Issue: 5 , May 1995
Pages:609 - 623

[Abstract] [PDF Full-Text (1408 KB)] **IEEE JNL**

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3 **A loop partition technique for reducing cache bank conflict in multithreaded architecture**
Wu, C.-C.; Chen, C.F.;
Computers and Digital Techniques, IEE Proceedings- , Volume: 143 , Issue: 1 , Jan. 1996
Pages:30 - 36

[Abstract] [PDF Full-Text (718 KB)] **IEE JNL**

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4 **Compiler algorithms for optimizing locality and parallelism on shared and distributed memory machines**
Kandemir, M.; Ramanujam, J.; Choudhary, A.;
Parallel Architectures and Compilation Techniques., 1997. Proceedings. 1997 International Conference on , 10-14 Nov. 1997
Pages:236 - 247

[Abstract] [PDF Full-Text (1116 KB)] **IEEE CNF**

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5 **Architectural and compiler support for energy reduction in the memory hierarchy of high performance microprocessors**
Hajj, N.B.M.; Polyckronopoulos, C.; Stamoulist, G.;
Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 10-12 Aug. 1998
Pages:70 - 75

[Abstract] [PDF Full-Text (524 KB)] **IEEE CNF**

6 **Bounds-based loop performance analysis: application to validation and tuning**
Bose, P.; Kim, S.; O'Connel, F.P.; Ciarfella, W.A.;
Performance, Computing and Communications, 1998. IPCCC '98., IEEE International , 16-18 Feb. 1998
Pages:178 - 184

[Abstract] [PDF Full-Text (596 KB)] **IEEE CNF**

7 **Software versus hardware coherence: performance versus cost**
Zucker, R.N.; Baer, J.-L.;
System Sciences, 1994. Vol. I: Architecture, Proceedings of the Twenty-Seventh Hawaii Internation Conference on , Volume: 1 , 4-7 Jan. 1994
Pages:163 - 172

[Abstract] [PDF Full-Text (648 KB)] **IEEE CNF**

8 **A three-million-transistor microprocessor**
Abu-Nofal, F.; Avra, R.; Bhabuthmal, K.; Bhamidipaty, R.; Blanck, G.; Charnas, A.; DelVecchio, P.; Grass, J.; Grinberg, J.; Hayes, N.; Haber, G.; Hunt, J.; Kizhepat, G.; Malamy, A.; Marston, A.; Mehta, K.; Nanda, S.; Van Nguyen, H.; Patel, R.; Ray, A.; Reaves, J.; Rogers, A.; Rusu, S.; Shay, T.; Sidharta, I.; Tham, T.; Tong, P.; Trauben, R.; Wong, A.; Yee, D.; Maan, N.; Steiss, D.; Youngs, L.;
Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC, 1992 IEEE International , 19-21 Feb. 1992
Pages:108 - 109, 257

[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

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